

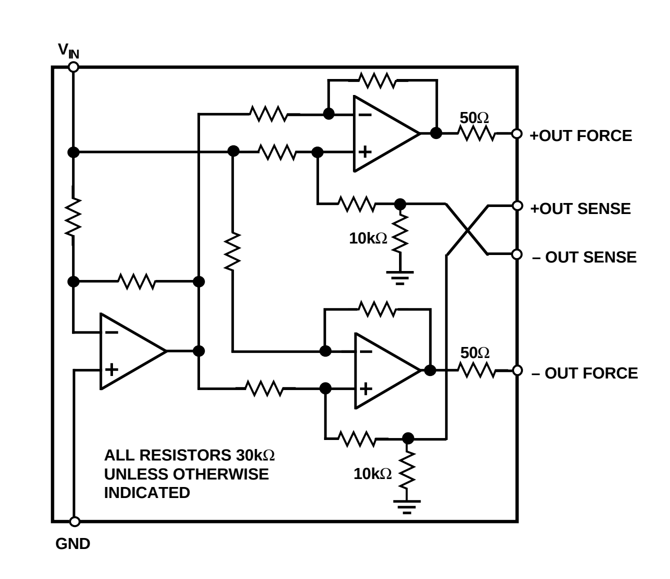
Balanced Line Driver

SSM2142

FEATURES
Transformer-Like Balanced Output
Drives 10 V RMS Into a 600 Ω Load
Stable When Driving Large Capacitive Loads and Long Cables
Low Distortion
0.006% typ 20 Hz–20 kHz, 10 V RMS into 600 Ω
High Slew Rate
15 V/µs typ
Low Gain Error
(Differential or Single-Ended); 0.7% typ
Outputs Short-Circuit Protected
Available In Space-Saving 8-Pin Mini-DIP Package
Low Cost

APPLICATIONS
Audio Mix Consoles
Distribution Amplifiers
Graphic and Parametric Equalizers
Dynamic Range Processors
Digital Effects Processors
Telecommunications Systems
Industrial Instrumentation
Hi-Fi Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The SSM2142 is an integrated differential-output buffer amplifier that converts a single-ended input signal to a balanced output signal pair with high output drive. By utilizing low noise thermally matched thin film resistors and high slew rate amplifiers, the SSM2142 helps maintain the sonic quality of audio systems by eliminating power line hum, RF interference, voltage drops, and other externally generated noise commonly encountered with long audio cable runs. Excellent rejection of common-mode noise and offset errors is achieved by laser trimming of the onboard resistors, assuring high gain accuracy. The carefully designed output stage of the SSM2142 is capable of driving difficult loads, yielding low distortion performance despite extremely long cables or loads as low as 600 Ω, and is stable over a wide range of operating conditions.

Based on a cross-coupled, electronically balanced topology, the SSM2142 mimics the performance of fully balanced transformer-based solutions for line driving. However, the SSM2142 maintains lower distortion and occupies much less board space than transformers while achieving comparable common-mode rejection performance with reduced parts count.

The SSM2142 in tandem with the SSM2141 differential receiver establishes a complete, reliable solution for driving and receiving audio signals over long cables. The SSM2141 features an Input Common-Mode Rejection Ratio of 100 dB at 60 Hz. Specifications demonstrating the performance of this typical system are included in the data sheet.

REV. B

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Tel: 617/329-4700 **Fax: 617/326-8703**

SSM2142–SPECIFICATIONS (V_S = ±18 V, –40°C ≤ T_A ≤ +85°C, operating in differential mode unless otherwise noted. Typical characteristics apply to operation at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT IMPEDANCE	Z_{IN}			10		kΩ
INPUT CURRENT	I_{IN}	V_{IN} = ±7.071 V		±750	±900	µA
GAIN, DIFFERENTIAL			5.8	5.98		dB
GAIN, SINGLE-ENDED		Single-Ended Mode	5.7	5.94		dB
GAIN ERROR, DIFFERENTIAL		R_L = 600 Ω		0.7	2	%
POWER SUPPLY REJECTION RATIO STATIC	PSRR	V_S = ±13 V to ±18 V	60	80		dB
OUTPUT COMMON-MODE REJECTION	OCMR	See Test Circuit; f = 1 kHz	–38	–45		dB
OUTPUT SIGNAL BALANCE RATIO	SBR	See Test Circuit; f = 1 kHz	–35	–40		dB
TOTAL HARMONIC DISTORTION Plus Noise	THD+N	20 Hz to 20 kHz, V_O = 10 V rms, R_L = 600 Ω		0.006		%
SIGNAL-TO-NOISE RATIO	SNR	V_{IN} = 0 V		–93.4		dBu
HEADROOM	HR	CLIP Level = 10.5 V rms		+93.4		dBu
SLEW RATE	SR			15		V/µs
OUTPUT COMMON-MODE VOLTAGE OFFSET[1]	V_{OOS}	R_L = 600 Ω	–250	25	250	mV
DIFFERENTIAL OUTPUT VOLTAGE OFFSET	V_{OOD}	R_L = 600 Ω	–50	15	50	mV
DIFFERENTIAL OUTPUT VOLTAGE SWING		V_{IN} = ±7.071 V	±13.8	±14.14		V
OUTPUT IMPEDANCE	Z_O		45	50	55	Ω
SUPPLY CURRENT	I_{SY}	Unloaded, V_{IN} = 0 V		5.5	7.0	mA
OUTPUT CURRENT, SHORT CIRCUIT	I_{SC}		60	70		mA

NOTES
[1]Output common-mode offset voltage can be removed by inserting dc blocking capacitors in the sense lines. See Applications Information.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . ±18 V
Storage Temperature . . . . –60°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . +300°C
Junction Temperature . . . . +150°C
Operating Temperature Range . . . . –40°C to +85°C
Output Short Circuit Duration (Both Outputs) . . . . Indefinite

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

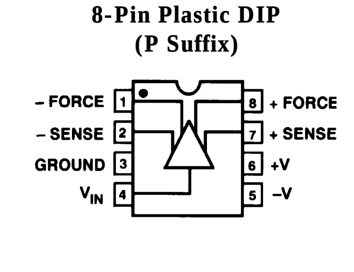
ORDERING GUIDE

Model	Operating Temperature Range	Package Description	Package Option
SSM2142P	–40°C to +85°C	Plastic DIP	N-8
SSM2142S*	–40°C to +85°C	SOL	R-16

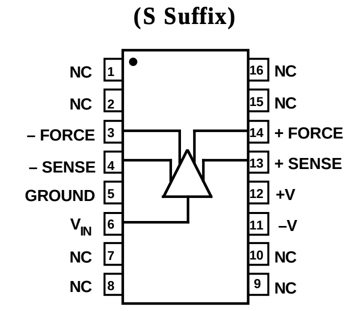
*For availability of SOIC package, contact your local sales office.

PIN CONNECTIONS

8-Pin Plastic DIP (P Suffix)



16-Pin Wide Body SOL (S Suffix)



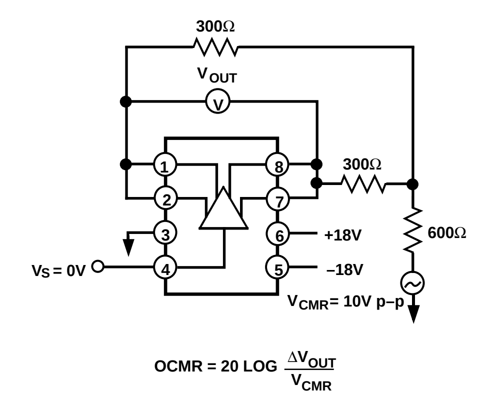


Figure 1. Output CMR Test Circuit

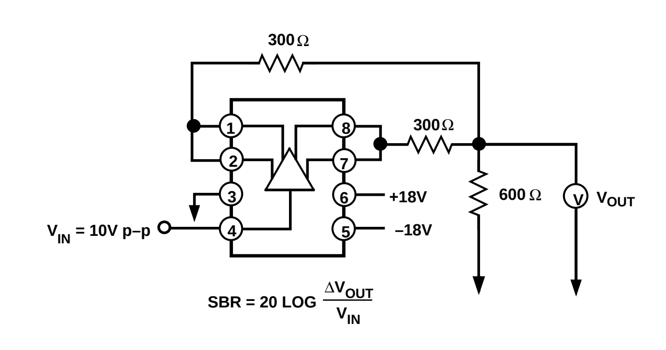


Figure 2. Signal Balance Ratio (BBC Method) Test Circuit

Typical Performance Characteristics

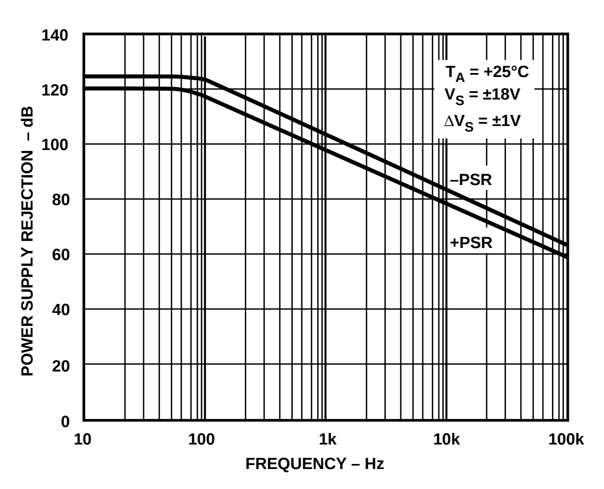


Figure 3. Power Supply Rejection vs. Frequency

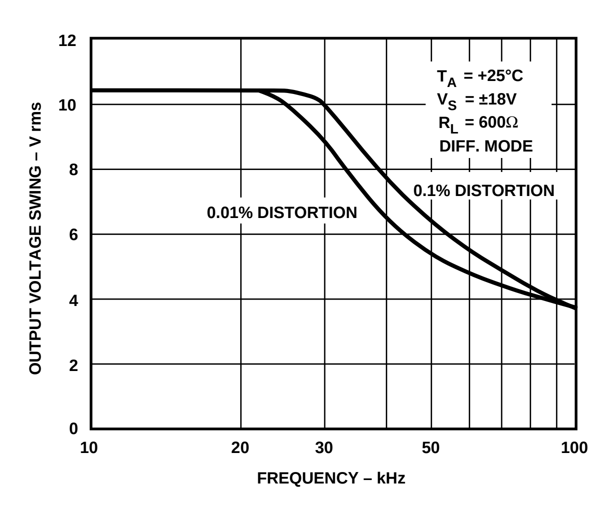


Figure 4. Maximum Output Voltage Swing vs. Frequency

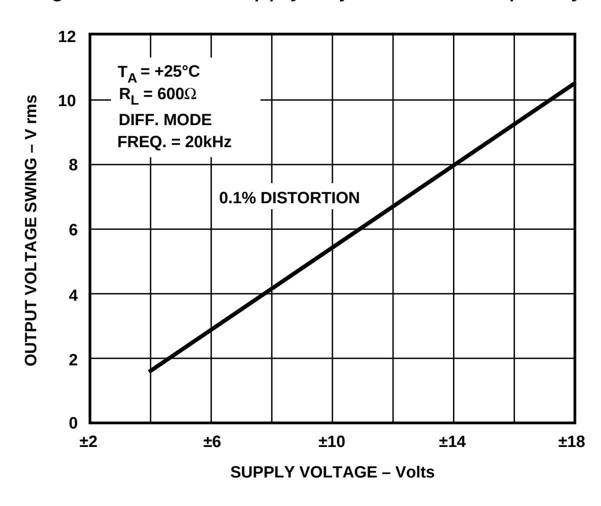


Figure 5. Output Voltage Swing vs. Supply Voltage

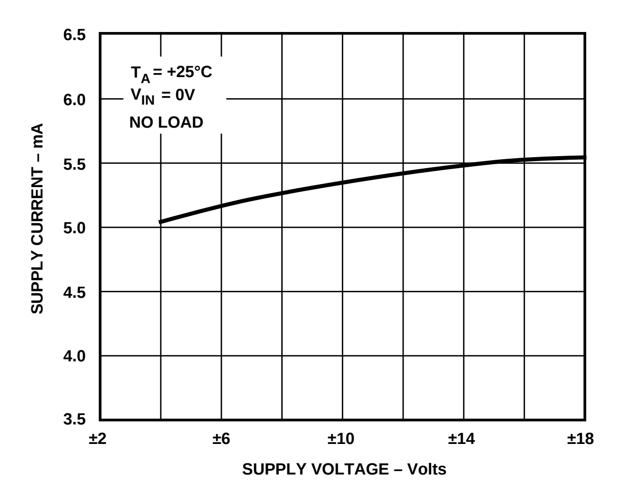
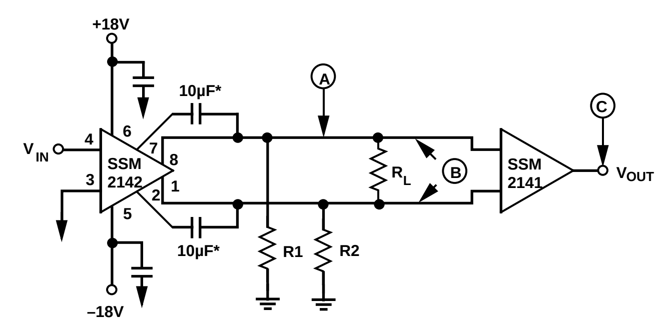


Figure 6. Supply Current vs. Supply Voltage

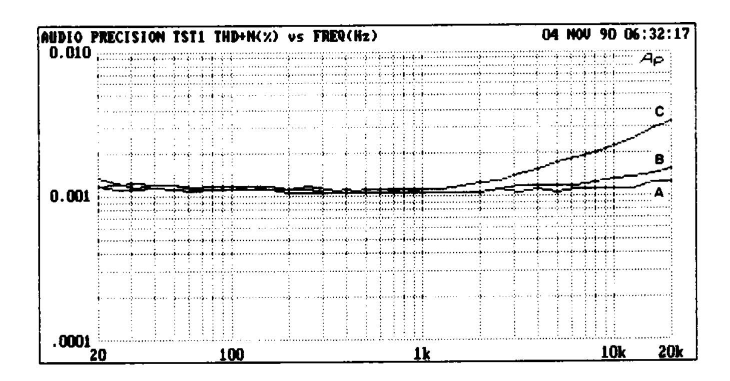
THD PERFORMANCE

The following data, taken from the THD test circuit on an Audio Precision System One using the internal 80 kHz noise filter, demonstrates the typical performance of a balanced pair system based on the SSM2142/SSM2141 chip set. Both differential and single-ended modes of operation are shown, under a number of output load conditions which simulate various application situations. Note also that there is no adverse effect on system performance when using the optional series feedback capacitors, which reject dc cable offsets in order to maintain optimal ac noise rejection. The large signal transient response of the system to a 100 kHz square wave input is also shown, demonstrating the stability of the SSM2142 under load.



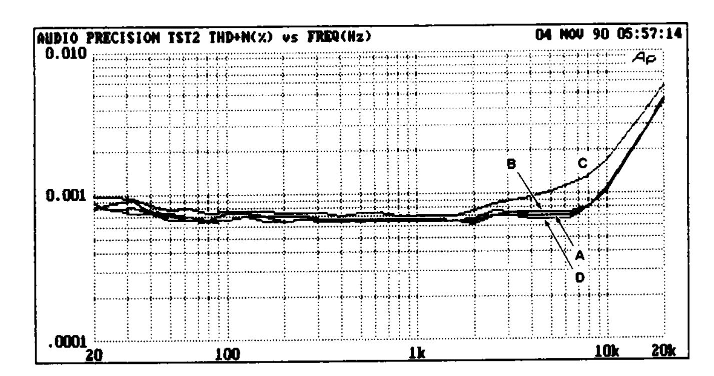
*USED ONLY IN THD PLOTS AS NOTED.
ALL CABLE MEASUREMENTS USE BELDEN 8451 CABLE.

Figure 7. THD Test Circuit



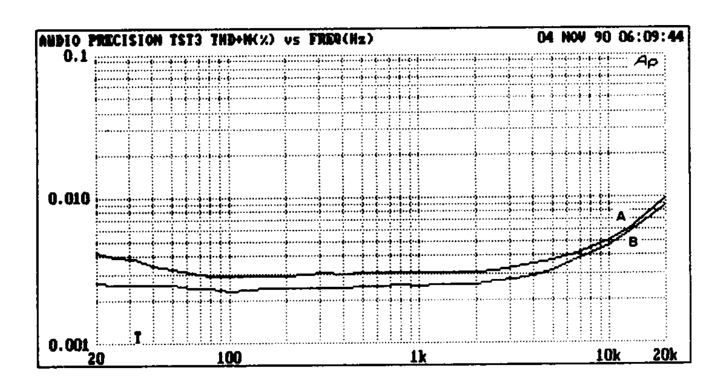
V_O = 10 V rms, NO CABLE
A: R1 = R2 = R_L = ∞
B: R1 = R2 = 600 Ω, R_L = ∞
C: R1 = R2 = ∞, R_L = 600 Ω

Figure 8. THD+N vs. Frequency at Point B (Differential Mode)



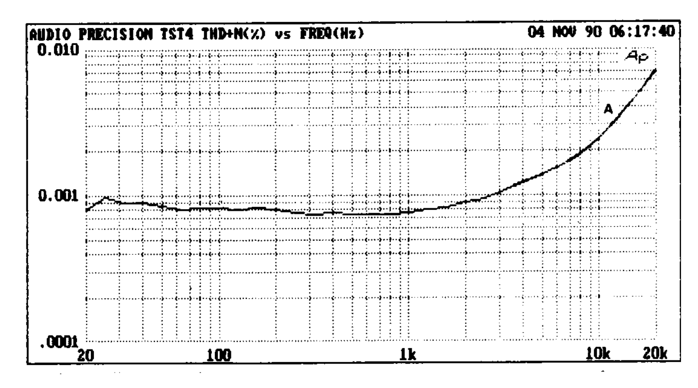
V_O = 10 V rms, WITH 500 FEET CABLE
A: R1 = R2 = R_L = ∞
B: R1 = R2 = 600 Ω, R_L = ∞
C: R1 = R2 = ∞, R_L = 600 Ω
D: R1 = R2 = R_L = ∞, WITH SERIES FEEDBACK CAPACITORS

Figure 9. THD+N vs. Frequency at Point B (Differential Mode)



V_O = 10 V rms, R2 = 0 Ω, R_L = ∞
A: R1 = 600 Ω, WITH 250 FEET CABLE
B: R1 = ∞, NO CABLE

Figure 10. THD+N vs. Frequency at Point A (Single Ended)



V_O = 10 V rms, NO CABLE
A: R1 = R2 = ∞, R_L = 600 Ω

Figure 11. THD+N vs. Frequency at Point C (SSM2141 Output)

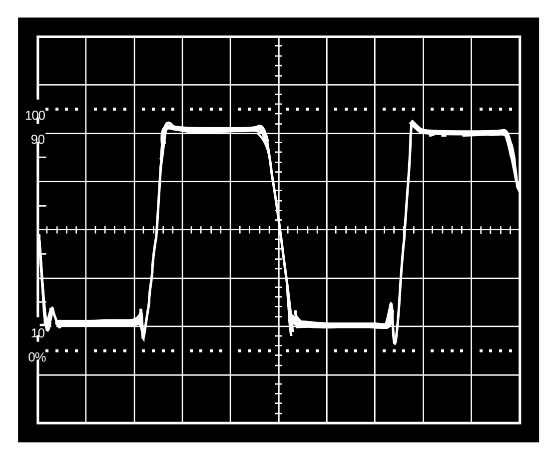


Figure 12. 100 kHz Square Wave Observed at Point B (Differential Mode). V_O = 10 V rms, R1 = R2 = ∞, R_L = 600 Ω

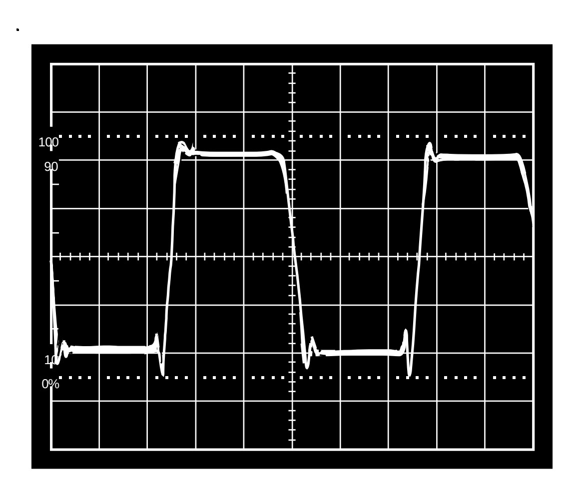


Figure 13. 100 kHz Square Wave at Point B (Differential Mode). V_O = 10 V rms, R1 = R2 = ∞, R_L = 600 Ω, with Series Feedback Capacitors

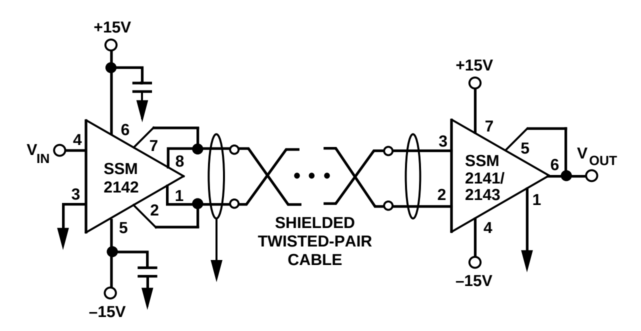


Figure 14. Typical Application of the SSM2142 and SSM2141

APPLICATIONS INFORMATION

The SSM2142 is designed to provide excellent common-mode rejection, high output drive, and low signal distortion and noise in a balanced line-driving system. The differential output stage consists of twin cross-coupled unity gain buffer amplifiers with on-chip 50 Ω series damping resistors. The impedances in the output buffer pair are precisely balanced by laser trimming during production. This results in the high gain accuracy needed to obtain good common-mode noise rejection, and excellent separation between the offset error voltages common to the cable pair and the desired differential input signal. As shown in the test circuit, it is suggested that a suitable balanced, high input-impedance differential amplifier such as the SSM2141 be used at the receiving end for best system performance. The SSM2141 receiver output is configured for a gain of one half following the 6 dB gain of the SSM2142, in order to maintain an overall system gain of unity.

In applications encountering a large dc offset on the cable or those wishing to ensure optimal rejection performance by avoiding differential offset error sources, dc blocking capacitors may be employed at the sense outputs of the SSM2142. As shown in the test circuit, these components should present as little impedance as possible to minimize low-frequency errors, such as 10 µF NP (or tantalum if the polarity of the offset is known).

SYSTEM GROUNDING CONSIDERATIONS

Due to ground currents, supply variations, and other factors, the ground potentials of the circuits at each end of a signal cable may not be exactly equal. The primary purpose of a balanced pair line is to reject this voltage difference, commonly called "longitudinal error." A measure of the ability of the system to reject longitudinal error voltage is output common-mode rejection. In order to obtain the optimal OCMR and noise rejection performance available with the SSM2142, the user should observe the following precautions:

1. The quality of the differential output is directly dependent upon the accuracy of the input voltage presented to the device. Input voltage errors developed across the impedance of the source must be avoided in order to maintain system performance. The input of the SSM2142 should be driven directly by an operational amplifier or buffer offering low source impedance and low noise.
2. The ground input should be in close proximity to the single-ended input's source common. Ground offset errors encountered in the source circuitry also impair system performance.
3. Make sure that the SSM2142 is adequately decoupled with 0.1 µF bypass capacitors located close to each supply pin.
4. Avoid the use of passive circuitry in series with the SSM2142 outputs. Any reactive difference in the line pair will cause significant imbalances and affect the gain error of the device. Snubber networks or series load resistors are not required to maintain stability in SSM2142 based systems, even when driving signals over extremely long cables.
5. Efforts should be made to maintain a physical balance in the arrangement of the signal pair wiring. Capacitive differences due to variations in routing or wire length may cause unequal noise pickup between the pair, which will degrade the system OCMR. Shielded twisted-pair cable is the preferred choice in all applications. The shield should not be utilized as a signal conductor. Grounding the shield at one end, near the output common, avoids ground loop currents flowing in the shield which increase noise coupling and longitudinal errors.

THE CABLE PAIR

The SSM2142 is capable of driving a 10 V rms signal into 600 Ω and will remain stable despite cable capacitances of up to 0.16 µF in either balanced or single-ended configurations. Low impedance shielded audio cable such as the standard Belden 8451 or similar is recommended, especially in applications traversing considerable distances. The user is cautioned that the so-called "audiophile" cables may incur four times the capacitance per unit length of the standard industrial-grade product. In situations of extreme load and/or distance, adding a second parallel cable allows the user to trade off half of the total line resistance against a doubling in capacitive load.

SINGLE-ENDED OPERATION

The SSM2142 is designed to be compatible with existing balanced-pair interface systems. Just as in transformer-based circuits, identical but opposite currents are generated by the output pair which can be ground-referenced if desired and transmitted on a single wire. Single-ended operation requires that the unused side of the output pair be grounded to a solid return path in order to avoid voltage offset errors at the nearby input common. The signal quality obtained in these systems is directly dependent on the quality of the ground at each end of the wire. Also note that in single-ended operation the gain through the device is still 6 dB, and that the SSM2142 incurs no significant degradation in signal distortion or output drive capability, although the noise rejection inherent in balanced-pair systems is lost.

POWER SUPPLY SEQUENCING

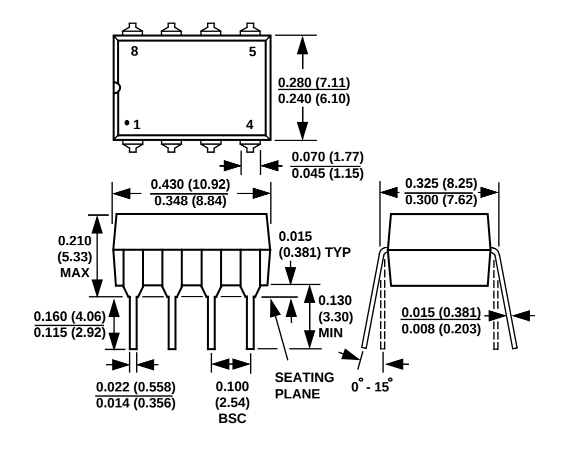
A problem occasionally encountered in the interface system environment involves irregular application of the supplies. The user is cautioned that applying power erratically can inadvertently bias parts of the circuit into a latch-up condition. The small geometries of an integrated circuit are easily breached and damaged by short-risetime spikes on a supply line, which usually demonstrate considerable overshoot. The questionable practice of exchanging components or boards while under power can create such an undesirable sequence as well. Possible options which offer improved board-level device protection include: additional bypass capacitors, high-current reverse-biased steering diodes between both supplies and ground, various transient surge suppression devices, and safety grounding connectors.

Likewise, power should be applied to the device before the output is connected to "live" systems which may carry voltages of sufficient magnitude to turn on the output devices of the SSM2142 and damage the device. In any case, of course, the user must always observe the absolute maximum ratings shown in the specifications.

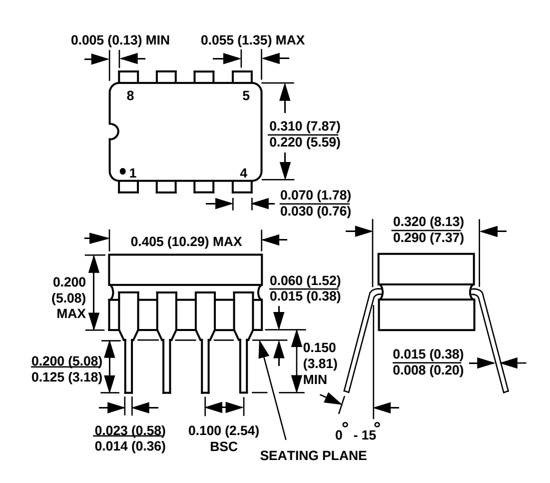
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

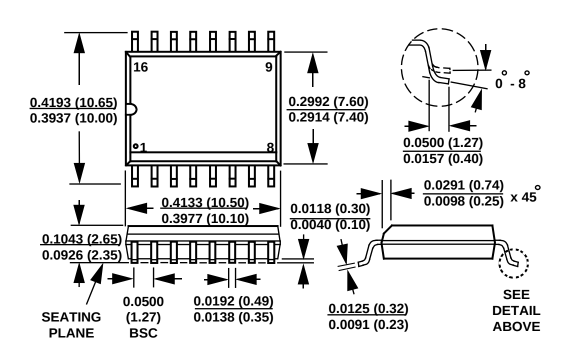
8-Lead Plastic DIP



8-Lead Cerdip



16-Lead Small Outline (SOIC)



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